

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Kiyoshi Kato Art Unit : Unknown  
Serial No. : New Application Examiner : Unknown  
Filed : April 27, 2006  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND DESIGN METHOD  
THEREOF

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

## **INFORMATION DISCLOSURE STATEMENT**

Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request.

Submitted herewith is an English translation of the following foreign language references, or portions thereof:

Desig. ID	Source
AP	JP11-154169 – English Abstract : esp@cenet database – Worldwide (2006)

This statement is being filed with the application. Please apply any charges or credits to  
Deposit Account No. 06-1050.

Respectfully submitted,

Date: April 27, 2006

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Substitute Form PTO-1449 (Modified)		U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-335US1	Application No.
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Kiyoshi Kato		
		Filing Date April 27, 2006	Group Art Unit	

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0083398 A1	06/27/2002	Takeyama et al.			03/30/2001
	AB	2003/0009727 A1	01/09/2003	Takeyama et al.			09/09/2002
	AC	2004/0232459 A1	11/25/2004	Takayama et al.			10/31/2003
	AD	2004/0238827 A1	12/02/2004	Takayama et al.			03/09/2004
	AE	2005/0250266 A1	11/10/2005	Yamazaki et al.			07/12/2005
	AF	5,705,829	01/06/1998	Miyanaga et al.			01/26/1996
	AG	5,939,731	08/17/1999	Yamazaki et al.			01/08/1997
	AH	6,034,675	03/07/2000	Yamazaki			07/03/1995
	AI	6,400,360 B1	06/04/2002	Yamazaki			01/03/2000
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	AM	6,697,059 B2	02/24/2004	Yamazaki			05/24/2002
	AN	6,955,954 B2	10/18/2005	Miyanaga et al.			12/30/2003
	AO	6,995,432 B2	02/07/2006	Yamazaki et al.			11/22/2002

**Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation
							Yes No
	AP	11-154169	06/08/1999	JAPAN			AB
	AQ						

**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AR	Buyeol Lee et al.; "A CPU on a Glass Substrate Using CG-Silicon TFTs"; <i>ISSCC 2003 / Session 9 / TD: Digital Architecture and Systems / Paper 9.4 (Digest of Technical Papers)</i> - <i>IEEE International Solid-State Circuits Conference Vol. 1</i> ; pp. 164-165; February 11, 2003
	AS	David Van Campenhout et al.; "Timing Verification of Sequential Dynamic Circuits"; <i>IEEE Transactions of Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No. 5</i> ; pp. 645-658; May 1999
	AT	International Search Report (Application No. PCT/JP2004/016174) dated January 25, 2005

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.Y.D.

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		Filing Date April 27, 2006	Group Art Unit

<b>Other Documents (include Author, Title, Date, and Place of Publication)</b>		
Examiner Initial	Desig. ID	Document
	AU	Written Opinion (Application No. PCT/JP2004/016174) dated January 25, 2005

Examiner Signature	/Magid Dimyan/	Date Considered	04/07/2008
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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